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6. The apparatus according to claim 5, wherein said ID code is combined with other identification codes.

7. The apparatus according to claim 6, wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacture number.

8. The apparatus according to claim 1, wherein said ID code is captured in a register.

9. The apparatus according to claim 8, wherein said register comprises a JTAG ID code register.

10. The apparatus according to claim 1, wherein said apparatus comprises a programmable logic device (PLD).

11. The apparatus according to claim 1, wherein said metal options are set to indicate an operating voltage of said apparatus.

13. The apparatus according to claim 1, wherein said pins are labeled as either a first or a second supply voltage.

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15. The apparatus according to claim 14, wherein said  
 stics comprise one or more characteristics selected from  
 consisting of volatility, price, and density.

16. A method of selecting one of a number of  
tion codes for a single die and package combination  
the steps of:

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(B) generating said one of a number of identification response to said voltage levels on said one or more pins.

17. The method according to claim 16, wherein the step (B) comprises the sub-steps of:

(B-1) determining said voltage levels;

(B-2) determining a state of one or more metal options;

(B-3) determining a state of one or more bond options; and

(B-4) generating an identification code in response to a logical combination of the determinations of sub-steps (B-1) through (B-2).

18. The method according to claim 16, further comprising the step of:

(C) presenting said identification code in response to an identification request.

19. The method according to claim 18, wherein said identification request comprises a JTAG ID code instruction.

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20. An apparatus comprising:

means for generating a number of identification codes in  
response to a voltage level asserted at one or more pins; and

means for determining a voltage level to assert at one or

5 more pins.

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